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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,317	10/23/2001	Michael Kowalchik	EMR-00401	2338

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EXAMINER	
CHACE, CHRISTIAN	

ART UNIT	PAPER NUMBER
2187	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,317	KOWALCHIK ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to Amendment filed 4 February 2004. Claims 1-38 are pending. Applicants' arguments have been carefully and respectfully considered in light of the instant amendment, but they are not persuasive. Accordingly, this action has been made FINAL, as necessitated by amendment.

Double Patenting

Copending applications 10/001,317 (instant) and 10/004,090 were found to have obviousness-type provisional double-patenting issues. 10/004,090 was found to have broader claims than the instant application.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 4, 5, and 23 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 4, and 20, respectively, of copending Application No. 10/004,090. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 4 and

5 of the instant application anticipate respective claims 1 and 4 of the copending application, and instant claim 23 is missing one limitation of copending application's claim 20, which is an obvious modification. All of this is explained below in detail.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

With respect to claims 4 and 5 of the instant application, please refer to the table below, which illustrates the anticipatory relationship of the claims at issue:

Instant Application 10/001,317	**Application 10/004,090**
4. A cache comprising:	**1**. A data storage device, the device comprising:
A front-end interface	A device interface
That receives data access requests	For receiving data access requests
That specify respective data storage addresses	[inherent: any storage access request must specify an address, or location, of the data or area it wishes to access]
A back-end interface that can retrieve data identified by the data storage address	
Cache storage formed by at least two disks	More than two disk drives
Cache manager	A controller
That services at least some of the requests	That accesses the disk drives
Received at the front-end interface	In response to the received data access requests
Using data stored in the cache storage	[inherent: by accessing the disk drives, data stored in the disk drives is "used."]
Wherein the disks comprise disks having platters less than 3.5 inches in diameter	[disk drives] having platter sizes less than 3.5 inches in diameter
5. (depends upon claim 4, so contains all of the limitations supra)	**4**. (depends on claim 1, so contains all of the limitations supra)
Wherein the disks comprise disks having at least one of the following platter sizes: 2.5 inches, 1.8 inches, and 1 inch in diameter	Wherein the platter sizes comprise platters of at least one of the following sizes: 2.5 inches, 1.8 inches, and 1 inch

Claim 23 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 20 of copending Application No. 10/004090 in view of *Modern Operating Systems,* Tanenbaum, page 306 (cited in IDS filed 10/23/01 in both applications). As will be illustrated below in the table, the instant claim 23 would anticipate copending claim 20, with the exception of the at least one first data storage device having a platter size of at least 3.5 inches in diameter.

Instant Application 10/001,317	**Application 10/004,090**
23. A data storage system, comprising:	**20.** A data storage system, the system comprising:
A back-end storage system	At least one first data storage device
having an address space, addresses in the address space identifying blocks of storage	[inherent: storage systems must have addresses and addresses inherently identify blocks of storage, or storage locations]
[Obvious: see *Graham v. Deer* factors below]	Having a platter size of at least 3.5 inches in diameter
A cache for the back-end storage system	At least one second data storage device
Having a lesser storage capacity than the back-end system	[inherent: definition of a cache, i.e., smaller and faster memory for faster access closer to the processor]
The cache including:	Comprising:
A front-end interface	A device interface
That receives I/O requests	For receiving data access requests
That specify respective addresses of back-end storage blocks	[inherent as discussed supra]
A back-end interface	A second controller
That communicates with the back-end storage system	That coordinates data access to the at least one first data storage device and the at least one second storage device
Cache storage formed by at least two disks having platter diameters less than 3.5 inches	More than two disk drives coupled to the controller, the drivers having platter sizes less than 3.5 inches in diameter
A cache manager that services at least some of the I/O requests received via the front-end interface using blocks temporarily stored in the cache storage	A first controller configured to receive data access requests from the interface

However, Tanenbaum discloses that CD ROM's are 120 millimeters across, which is more than 3.5 inches, in the second paragraph of page 306.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the instant application and Tanenbaum before him/her, to have a back-end storage device (first data storage device) with platter sizes of at least 3.5 inches, as CD ROMS are at least 3.5 inches, and they have much higher recording densities than conventional magnetic disks, as disclosed by Tanenbaum in line 2 of the second paragraph on page 306.

This is a provisional obviousness-type double patenting rejection.

Claim Objections

Claims 24, 27, 29, and 33 are objected to because of the following informalities: "...simultaneously access[ing] and retriev[ing] the data stored on said at least two disks..." is confusing. It is unclear whether the accessing and retrieving is done at the same time per disk, or that the accessing is done on all disks at the same time, and then the retrieving is done on all disks at the same time. Also, retrieving IS accessing. For the purposes of examination, examiner has interpreted this as the latter, or, in other words, parallel access to the disks by striping, for example. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Brant et al (US Patent #5,805,787).

With respect to independent claim 1, a cache is disclosed in the title and abstract (#16 in figure 1). A cache is, by definition, a memory subsystem in which frequently used values are duplicated for quick access. A cache stores the contents of frequently accessed main memory locations and the addresses where these data items are stored in the main memory. A cache is useful between a processor and a main memory when main memory accesses are slow compared to the processor speed, because the cache memory is always faster than the main memory.

A front-end interface is disclosed in figure 1, #11, as the "host interface" in column 6, line 17.

A back-end interface is disclosed in figure 1 as #24, as the "interface to the mass data storage subsystem" in column 6, line 18.

Cache storage being formed by at least two disks is disclosed in figure 1, #16, and discussed in the abstract, for example.

A cache manager is disclosed as the storage controller in figure 1, #20. As discussed in column 4, lines 9-19, the storage controller receives data access requests

(via front-end interface #11) that specify respective data storage addresses, retrieves data identified by the data storage addresses, and services at least one of the requests received at the front-end interface using data stored said at least two disks. The at least one of the requests serviced are, of course, the ones in which the cache holds the information for. As the definition of cache suggests, as discussed supra, if the cache does not have the information, the cache does not service the request *per se*, but the main memory, or larger storage does (via back-end interface #24). This is also discussed in column 4, lines 9-19. As the data stored in the at least two disks that make up the cache is stored striped in a RAID configuration, as discussed in column 5, lines 34, 36, and 44, for example. This is significant as RAID 3, for example, as mentioned in column 5, line 44, adds redundant information in the form of parity to a parallel access striped array, by definition. Striping is assigning blocks of storage in regular sequence to all of an array's disks. Therefore, Brant et al uses stores the data in the at least two disks that make up the cache by striping it in a RAID 3 configuration, for example.

With respect to claims 2 and 15, the front-end interface comprising an interface conforming to "a protocol" is disclosed in column 6, lines 39-41, for example, where the protocol is a "SCSI-type connection[s].".

With respect to claims 3 and 16, the protocol comprising at least one of SCSI, Fibre Channel, "INFINIBAND," and IDE is disclosed in column 6, line 22, which identifies IDE, as well as line 41, which identifies SCSI and associates SCSI with the front-end interface (host interface #11).

With respect to claim 4, the disks comprising disks having platters less than 3.5 inches in diameter is disclosed in column 3, lines 44-46.

With respect to claim 5, the disks comprising disks having at least one of the following platter sizes: 2.5 inches, 1.8 inches, and 1 inch in diameter is disclosed in column 3, lines 44-46, which not only discloses the 1.8 inch diameter disk, but also states that "(or smaller)" [would work in the invention]. "Or smaller" would include the 1 inch diameter as well.

With respect to claims 6 and 19, the cache implementing a RAID scheme using the disks is disclosed in column 5, lines 34, 36, and 44, in general. RAID stands for, "Redundant Array of Independent Disks." In this case, column 5, line 59 recites, "Controller 20 can include independent paths to write data to its memory in a mirrored fashion." Mirroring is redundant storage of data. The cache being an Array is disclosed in column 4, line 15, for example. Figure 1 clearly shows separate disks, and, therefore, independent disks. Therefore, RAID is explicitly disclosed embodied in the invention of Brant et al.

With respect to claim 7, the cache performing at least one of the following operations is disclosed below. Examiner reminds applicants that as the claim language stands, only one of the following limitations are required to be anticipated by the instant prior art of record. However, it happens that all of the following limitations are anticipated by the cited prior art of record as follows:

Requesting data from a back-end storage system (see column 6, lines 50-51);

Retrieving requested data from the [at least two] disks [making up the cache] (see column 4, lines 9-19);

Sending data to the back-end system for writing (column 6,lines 50-51);

Determining the location of back-end system data within the [at least two] disks [making up the cache] (column 4, lines 32-48).

Removing data from the [at least two] disks [making up the cache] (column 4, lines 42-44).

With respect to claim 8, the addresses specifying storage locations of a back-end storage system that includes a collection of one or more disks is disclosed in the definition of a cache, discussed supra, in that, "A cache stores the contents of frequently accessed main memory locations and the addresses where these data items are stored in the main memory." The back-end storage system is the main memory. The back-end storage system comprising a collection of one or more disks is disclosed in figure 1, #25 and further discussed in column 6, lines 57-58, for example.

With respect to claim 9, the requests comprising I/O requests is disclosed in column 5, line 35, which refers to I/O rates. An I/O rate must be calculated from I/O requests. Therefore, I/O requests are inherent in a system with an I/O rate being measured. Also, it is important to note that I/O is "Input/Output," which is defined as the complementary tasks of gathering data for a computer or program to work with, and of making the results of the computer's activities available to the user or to other computer processes. This is exactly what figure 1 shows – data is gathered from the disk-based disk cache and supplied to the host.

With respect to claims 10 and 21, the data storage addresses comprising data storage addresses within an address space is inherent by definition of an address, which merely denotes a location of memory in which something is, or may be, stored. The address space is the disk-based disk cache.

With respect to claims 11 and 22, the address space comprising an address space of back-end storage is disclosed by the definition of a cache, as discussed with respect to claims 1 and 8, for example.

With respect to claim 12, a storage hierarchy associated with the various contemporary storage configurations, in order of accessing speed, in column 5, lines 10-28. Column 5, lines 29-31, recites that, "A storage subsystem that has the MB cost of disk coupled with the performance of many disks operated in parallel can fill several intermediate slots in this hierarchy." By introducing the storage subsystem at another slot of the hierarchy that has a level below it of slower access storage, the subsystem effectively becomes another cache, and it's respective address space becomes another cache's address space. An example of another level of memory that would have a slower access time might be a tape library or the like.

With respect to claim 13, the cache storage having more than one disk spindle is inherent in a duplex mirrored disk subsystem, which is disclosed in column 3, line 1. A disk spindle is an axle for mounting a disk. A duplex disk subsystem is a system of two spindles, one of which is active while the other remains on standby, ready to take over processing if the active spindle malfunctions.

With respect to independent claim 14, receiving data access requests at the cache is disclosed in column 4, lines 32-41.

The cache having storage formed by at least two disks is disclosed in figure 1, #16, and discussed in the abstract, for example.

The requests specifying respective data storage addresses is disclosed in the title and abstract. A cache is, by definition, a memory subsystem in which frequently used values are duplicated for quick access. A cache stores the contents of frequently accessed main memory locations and the addresses where these data items are stored in the main memory. A cache is useful between a processor and a main memory when main memory accesses are slow compared to the processor speed, because the cache memory is always faster than the main memory.

As discussed in column 4, lines 9-19, the storage controller receives data access requests (via front-end interface #11) that specify respective data storage addresses, retrieves data identified by the data storage addresses, and services at least one of the requests received at the front-end interface using data stored in the at least two disks. The at least one of the requests serviced are, of course, the ones in which the cache holds the information for. As the definition of cache suggests, as discussed supra, if the cache does not have the information, the cache does not service the request *per se*, but the main memory, or larger storage does (via back-end interface #24). This is also discussed in column 4, lines 9-19. As the data stored in the at least two disks that make up the cache is stored striped in a RAID configuration, as discussed in column 5, lines 34, 36, and 44, for example. This is significant as RAID 3, for example, as mentioned in

column 5, line 44, adds redundant information in the form of parity to a parallel access striped array, by definition. Striping is assigning blocks of storage in regular sequence to all of an array's disks. Therefore, Brant et al uses stores the data in the at least two disks that make up the cache by striping it in a RAID 3 configuration, for example.

With respect to claim 17, the requests comprising at least one read request is disclosed in column 4, line 25, for example.

With respect to claim 18, servicing the requests comprising retrieving data from the back-end storage (main memory) and storing the data in at least one of the disks is inherent in the definition of caching. The addresses specifying storage locations of a back-end storage system that includes a collection of one or more disks is disclosed in the definition of a cache, discussed supra, in that, "A cache stores the contents of frequently accessed main memory locations and the addresses where these data items are stored in the main memory." The back-end storage system is the main memory. The back-end storage system comprising a collection of one or more disks is disclosed in figure 1, #25 and further discussed in column 6, lines 57-58, for example.

With respect to claim 20, servicing the requests comprising determining whether the collection of disks currently stores the requested data is disclosed in column 4, lines 39-41, for example.

With respect to independent claim 23, a data storage system is disclosed in figure 1.

A 'back-end' storage system is disclosed in figure 1, #25. Data storage spaces all have addresses, or locations for storing data – this is inherent, by definition of an

address and by definition of data storage. The addresses identifying "blocks" of storage is also inherent – a block of storage may be any size, as applicants have not limited such size in the instant claim. Therefore, examiner interprets a "block" to be one memory location.

A cache for the back-end storage system is disclosed in figure 1 as #16 as well as in the title and abstract. A cache is, by definition, a memory subsystem in which frequently used values are duplicated for quick access. A cache stores the contents of frequently accessed main memory locations and the addresses where these data items are stored in the main memory. A cache is useful between a processor and a main memory when main memory accesses are slow compared to the processor speed, because the cache memory is always faster than the main memory.

A front-end interface is disclosed in figure 1, #11, as the "host interface" in column 6, line 17. Receiving I/O requests that specify respective addresses of back-end storage blocks is disclosed in column 5, line 35, which refers to I/O rates. An I/O rate must be calculated from I/O requests. Therefore, I/O requests are inherent in a system with an I/O rate being measured. Also, it is important to note that I/O is "Input/Output," which is defined as the complementary tasks of gathering data for a computer or program to work with, and of making the results of the computer's activities available to the user or to other computer processes. This is exactly what figure 1 shows – data is gathered from the disk-based disk cache and supplied to the host.

A back-end interface is disclosed in figure 1 as #24, as the "interface to the mass data storage subsystem" in column 6, line 18.

Cache storage being formed by at least two disks is disclosed in figure 1, #16, and discussed in the abstract, for example. The disks having platter diameters [of] less than 3.5 inches is disclosed in column 3, lines 45-46.

A cache manager is disclosed as the storage controller in figure 1, #20. As discussed in column 4, lines 9-19, the storage controller receives data access requests (via front-end interface #11) that specify respective data storage addresses, retrieves data identified by the data storage addresses, and services at least one of the I/O requests received at the front-end interface using data stored in the cache storage. The at least one of the requests serviced are, of course, the ones in which the cache holds the information for. As the definition of cache suggests, as discussed supra, if the cache does not have the information, the cache does not service the request *per se*, but the main memory, or larger storage does (via back-end interface #24). This is also discussed in column 4, lines 9-19. As the data stored in the at least two disks that make up the cache is stored striped in a RAID configuration, as discussed in column 5, lines 34, 36, and 44, for example. This is significant as RAID 3, for example, as mentioned in column 5, line 44, adds redundant information in the form of parity to a parallel access striped array, by definition. Striping is assigning blocks of storage in regular sequence to all of an array's disks. Therefore, Brant et al uses stores the data in the at least two disks that make up the cache by striping it in a RAID 3 configuration, for example.

With respect to claims 24, 27, 29, and 33, the cache manager simultaneously accessing and retrieving the blocks for the at least one [I/O] request from said at least two disks in inherent in striping, as discussed supra with respect to the claims upon

which the instant claims depend. Examiner notes that proof of this inherency, offered solely as extrinsic evidence, is given in the instant specification at lines 16-24 of page 6 amidst a discussion of striping in RAID.

With respect to claims 25, 30, and 37, the cache further comprising at least one interface conforming to a protocol to allow at least one additional disk to be connected to said storage is disclosed in column 6, lines 39-41, for example, where the protocol is a SCSI-type connection(s). A SCSI interface is inherently used to connect CPU's or hosts to SCSI peripheral devices (note the plural), such as many hard disks and printers, using SCSI ports, which inherently provide logical connections between the computer and all of the devices on the SCSI bus. Therefore, inherently, a SCSI bus connection through SCSI ports allows at least one additional disk to be connected through the interface.

With respect to claims 26, 28, 31, and 38, the cache manager storing identification data identifying addresses within said cache storage where data is stored and the corresponding address at a back-end storage area where data is stored is inherent in a direct-mapped strategy, as discussed in column 7, lines 35-40, which discusses a certain number of bits describing the address of the main store and a certain number of bits describing the location in the cache.

With respect to independent claim 32, a data storage system is disclosed in figure 1.

A 'back-end' storage system is disclosed in figure 1, #25. Data storage spaces all have addresses, or locations for storing data – this is inherent, by definition of an address and by definition of data storage. The addresses identifying "blocks" of storage

is also inherent – a block of storage may be any size, as applicants have not limited such size in the instant claim. Therefore, examiner interprets a "block" to be one memory location.

A plurality of caches is disclosed in column 5, lines 29-31, which discusses that the invention of Brant et al may be put in any multiple locations in the hierarchy of the system. Inherently, if the Brant et al invention is placed in "back-to-back" locations, if you will, then the front end interface of one of the locations will connect to the back-end interface of the next. Indeed, this is the definition of a hierarchical memory scheme. Inherently, each level stores less than the main memory, or back-end storage system, by definition. The back-end storage system is disclosed in figure 1 as #16 as well as in the title and abstract. A cache is, by definition, a memory subsystem in which frequently used values are duplicated for quick access. A cache stores the contents of frequently accessed main memory locations and the addresses where these data items are stored in the main memory. A cache is useful between a processor and a main memory when main memory accesses are slow compared to the processor speed, because the cache memory is always faster than the main memory.

A front-end interface is disclosed in figure 1, #11, as the "host interface" in column 6, line 17. Receiving I/O requests that specify respective addresses of back-end storage blocks is disclosed in column 5, line 35, which refers to I/O rates. An I/O rate must be calculated from I/O requests. Therefore, I/O requests are inherent in a system with an I/O rate being measured. Also, it is important to note that I/O is "Input/Output," which is defined as the complementary tasks of gathering data for a

computer or program to work with, and of making the results of the computer's activities available to the user or to other computer processes. This is exactly what figure 1 shows – data is gathered from the disk-based disk cache and supplied to the host.

A back-end interface is disclosed in figure 1 as #24, as the "interface to the mass data storage subsystem" in column 6, line 18.

Cache storage being formed by at least two disks is disclosed in figure 1, #16, and discussed in the abstract, for example. The disks having platter diameters [of] less than 3.5 inches is disclosed in column 3, lines 45-46.

A cache manager is disclosed as the storage controller in figure 1, #20. As discussed in column 4, lines 9-19, the storage controller receives data access requests (via front-end interface #11) that specify respective data storage addresses, retrieves data identified by the data storage addresses, and services at least one of the I/O requests received at the front-end interface using data stored in the cache storage. The at least one of the requests serviced are, of course, the ones in which the cache holds the information for. As the definition of cache suggests, as discussed supra, if the cache does not have the information, the cache does not service the request *per se*, but the main memory, or larger storage does (via back-end interface #24). This is also discussed in column 4, lines 9-19. As the data stored in the at least two disks that make up the cache is stored striped in a RAID configuration, as discussed in column 5, lines 34, 36, and 44, for example. This is significant as RAID 3, for example, as mentioned in column 5, line 44, adds redundant information in the form of parity to a parallel access striped array, by definition. Striping is assigning blocks of storage in regular sequence

to all of an array's disks. Therefore, Brant et al uses stores the data in the at least two disks that make up the cache by striping it in a RAID 3 configuration, for example.

With respect to claim 34, the plurality of caches being connected in series such that the front-end interface of one of said plurality of caches is coupled to the back-end interface of another of said plurality of caches is discussed supra with respect to claim 32. A plurality of caches is disclosed in column 5, lines 29-31, which discusses that the invention of Brant et al may be put in any multiple locations in the hierarchy of the system. Inherently, if the Brant et al invention is placed in "back-to-back" locations, if you will, then the front end interface of one of the locations will connect to the back-end interface of the next. Indeed, this is the definition of a hierarchical memory scheme.

Also inherent in the hierarchical scheme discussed supra, the front-end interface of the highest level cache would inherently connect to the host, while the back-end interface of the lowest-level cache would have to connect tot eh back-end storage system. This again, is by definition of hierarchical memory system.

With respect to claim 35, whereupon receiving one of [the] I/O requests at said front-end interface of one of the plurality of caches, the cache manager of said one of said plurality of caches sends data corresponding to said one of [the] I/O requests to said device making said one of [the] I/O requests if data is stored on the cache storage of said one of [said] plurality of caches is inherent, as it is the definition of a cache. All the instant claim recites is that if the requested data is in the cache, the cache sends the data to the host.

With respect to claim 36, whereupon receiving one of [the] I/O requests at said front-end interface of said one of said plurality of caches, the cache manager of said one of [said] plurality of caches sends said one of [said] I/O requests to one of said back-end storage [device] and another of said plurality of caches coupled to the back-end interface of said one of [said] plurality of caches if data is not stored on [in] the cache storage of said one of said plurality of caches is inherent in a hierarchical memory system, as discussed supra. The instant claim merely recites going to the next level cache if the data is not found in the first-level cache. This is how a hierarchical system such as the one discussed supra must operate.

Response to Arguments

With respect to the issue of double-patenting, while applicants may wish to delay the issue of the filing of a terminal disclaimer, as long as the provisional rejection is appropriate and proper, it will be repeated in the Office action, instantly and if any in the future.

With respect to applicants amendments tot eh specification, objections with respect to same have been withdrawn. Applicants' attention is, however, drawn to the objections to the claims, as discussed supra, and necessitated by amendment.

With respect to applicants' argument that Brant et al does not disclose a cache manager that services at least one of the requests using data stored on at least two disks, examiner respectfully disagrees. As explained supra with respect to instantly amended independent claims 1, 14, 23, and 32, for example, by using a striping RAID,

requested data is inherently on at least two disks, provided there are at least two disks in the system, which there are, as disclosed in figure 1, for example.

Examiner also wishes to refer applicants to MPEP 2144.04, B., which addresses the case of mere duplication of parts having no patentable significance unless a new and unexpected result is produced. As discussed supra, a new and unexpected result is not produced. In fact, it is inherent in the instant prior art as hierarchical structure is disclosed. Figure 8 of the instant disclosure, embodied in claims 32 and all that depend therefrom, merely show duplication of the claimed cache system. Although moot as a result of the inherency discussed supra, examiner finds that a discussion of such sections of MPEP may be helpful as applicants decide the future of prosecution of the instant application.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 703.306.5903. The examiner can normally be reached on 9-4-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703.308.1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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